REMARKS

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

Drawings Objections

The Examiner has objected to Fig. 3 as failing to comply with 37 C.F.R. § 1.84(p)(5) because the reference numbers are not clearly identified properly. Applicant has amended the figure to more clearly indicate the aforementioned reference numbers. A replacement sheet is attached hereto.

Specification Objections

The Examiner has objected to the disclosure because of the following informalities: In the specification on page 8, line 16, Fig. 2A is described. However there is no drawing identifying Fig. 2A. Applicant concurs. This figure should have been identified as Fig. 2. Applicant has amended the specification to correct this figure designation.

Rejection under 35 U.S.C. § 102

Claims 1-15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Akram, et al. (U.S. Patent No. 6,815,251). Applicant respectfully traverses this rejection.

Akram teaches a high density multi-chip having a plurality of integrated circuit dice with a row of central bond pads bonded in a staggered flip-chip style to opposite sides of a metallized substrate. Akram, Abstract; Figs. 5-8 and 12-15. The problem Akram attempts to solve is the attachment of chips *to opposite sides of a substrate*.

> Stacked groups of packaged devices, often called cubes, have been developed ... In these references, each non-conductive substrate has one or more IC dies attached to one side only, or when dies are attached to both sides of the substrate, not more than one die is so attached on its active surface.

Akram, Col. 1, ll.44-54.

Akram teaches, suggests, and discloses at least two die on opposite sides of a substrate in a staggered position.

> An exemplary embodiment of the invention is illustrated in drawing FIGS. 1 through 8 and is shown as a high density module 10 having two IC dies 12A, 12B mounted on a first side 16 of a substrate 20. One IC die 14A is shown on the opposite (second) side 18 of the substrate, in a staggered position relative to the dies 12A, 12B.

Akram, Col. 3, ll.46-52.

In the present invention, devices are stacked on top of one another in a staggered fashion on one side of a substrate. A first row of center bus memory chips are bonded face down to the substrate with the electrical connections maintained through an aperture or window in the substrate. Specification, p.7, ll.24-27. Importantly, the invention includes upper level chip(s) mounted to the lower chip(s), offset in a single axis such that the upper chip's center wire bond is exposed. Electrical connection of the upper chip is by bonding to the edge of the lower chip substrate. Specification, p.8, ll.1-3; Fig. 2. Akram does not teach, disclose, or suggest this die stacking configuration on a single side of the substrate, or the associated electrical

connections for the upper level chips. Specifically, as taught by claim 1 of the instant invention, Akram does not teach "a first upper layer memory device stack *on top of said first lower layer memory device* such that said first upper layer memory device is offset over said first lower layer memory device". Claim 1 (emphasis added).

Applicant has amended the independent claims to further clarify that the first upper layer memory device is bonded directly to the top of the first lower layer memory device as indicated in the specification:

> In order to achieve this placement, *the first top layer device 208 is seated on the first lower layer device 202* such that the top layer device's outer edge 210 is about at the center of the lower layer device.

Specification, p.8, l.29 – p.9, l.1 (emphasis added).

As shown in Figs. 2 and 3, the upper layer memory devices are bonded directly to the lower layer memory devices. Akram does not teach this. Applicant has amended claims 1, 7, and 10 to include having the first upper layer memory device seated on top of the first lower layer memory device, and bonded directly thereto.

It is respectfully submitted that the application has now been brought into a condition where allowance of the entire case is proper. Reconsideration and issuance of a notice of allowance are respectfully solicited.

Respectfully submitted,

Robert Curcio
Reg. No. 44,638

DeLIO & PETERSON, LLC
121 Whitney Avenue
New Haven, CT 06510-1241
(203) 787-0595

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Name: Barbara Browne Date: December 14, 2005 Signature:

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